DOUBLE BALANCED, COPLANAR, IMAGE REJECTION MIXER USES MONOLITHIC MESFET QUAD

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ABSTRACT

A coplanar double balanced image rejection mixer with an input 1 dB compression level of +10 dBm uses two MESFET ring quads with only +10 dBm LO power. This is considerably more efficient in terms of LO power when compared to Schottky diodes. Eigen-circuits are used to model the balun performance.

GENERAL

The current availability of economical low noise MMIC RF preamplifiers has increased the need for higher power level 2nd stage image (noise) rejection mixers. The increase in communication band signal densities and radar band jamming techniques has also focused system design attention on the upper limits of mixer dynamic range such as IP2, IP3. Conventional Schottky diode mixers typically require a ratio of at least 5 dB between input 1 dB compression point and P(LO) in order to avoid the RF input signal level from modulating the diode conductance and contributing to single and multitone intermod products. It is well known that MESFET mixers are less affected by RF signal power applied across the drain-source channel with the LO at the gate electrode (1). An extension of recent FET mixer technology (2) has resulted in a planar high level image rejection mixer for the popular 2.6 to 5.2 GHz intermediate frequency range. The circuit (see Figures 1, 3) employs coplanar construction for the 0° and 90° hybrids as well as the double balanced mixer baluns. Coplanar construction offers cost advantages since all assembly operations are on one face (no via holes). In addition, it is particularly convenient to interface several coplanar drop-in modules in a MIC assembly because the ground connections are also accessible from the topside and thus easily inspectable. Figure 2 shows the subsystem that this mixer was used in.

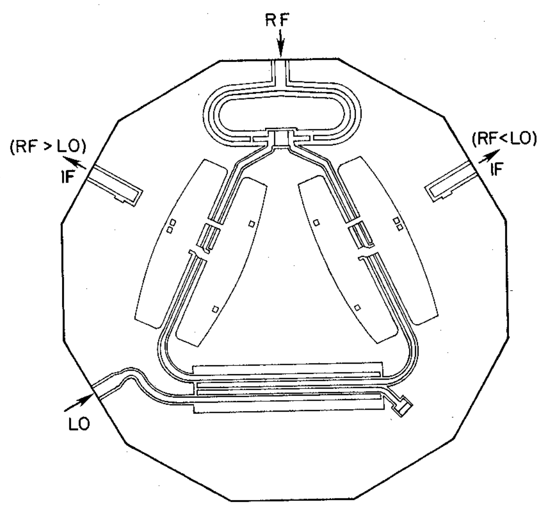

Figure 1: Coplanar Artwork for dB MESFET, Image Rejection Mixer.

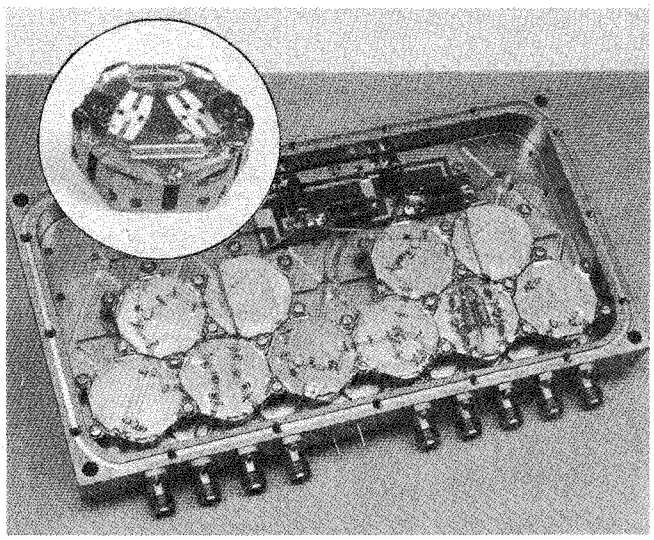

Figure 2: Subsystem Employing "CMIC" (Coplanar Microwave Integrated Circuit) Modules.

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The common hexagonal shape of each module was an experimental technique to lower subsystem development costs while maintaining maximum topology freedom. This construction technique has been nicknamed CMIC by RHG (Coplanar Microwave Integrated Circuit). Further work is being done using more conventional square coplanar module shapes.

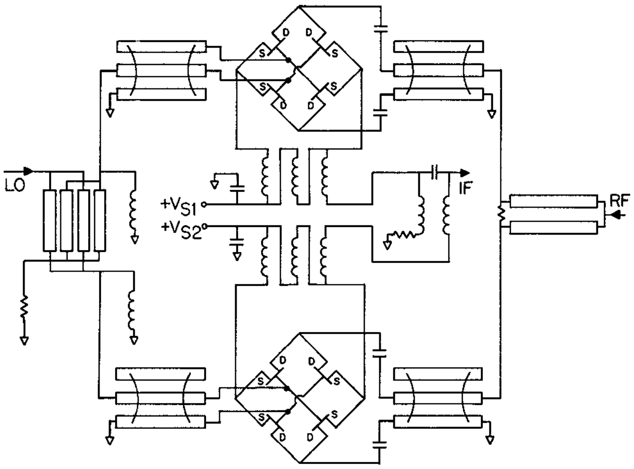

Figure 3: Schematic Diagram of Image Rejection Mixer Including Lumped Circuit IF Balun and Hybrid. (Mounted Under Substrate)

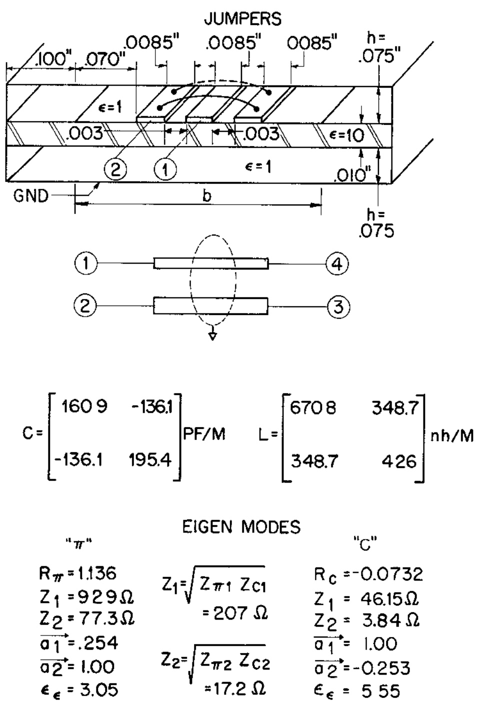

Figure 4a: Static L/C Parameters of Coplanar Balun.

COPLANAR BALUN AND COPLANAR DESIGN

Figure 4a shows the geometry and L/C matrix of the three strip conductor configuration based upon a static capacitance model (3). The TEM performance of the interdigital quadrature coupler was modeled on Touchstone using an asymmetric and nonhomogeneous network identity previously reported (4) which we refer to as the eigen-circuit. Figure 4b shows the equivalent 4 port decoupled model of the asymmetric lines derived from the mode voltage ratios of Tripathi (5). The balun has 3 lines but each outer line is common so its really 2 coupled lines. Similarly the quadrature coupler has 4 lines arranged as 1 interdigital equivalent symmetric pair. Figure 5 shows the amplitude and phase unbalance for the balun network including the effect of the unequal mode velocities. The advantage of the equivalent network is that one can inspect the flow graph of an nonhomogeneous and asymmetric microwave circuit and more easily make intuitive judgements about how to improve performance. The circuit is particularly helpful for estimating the effects of even-mode loading.

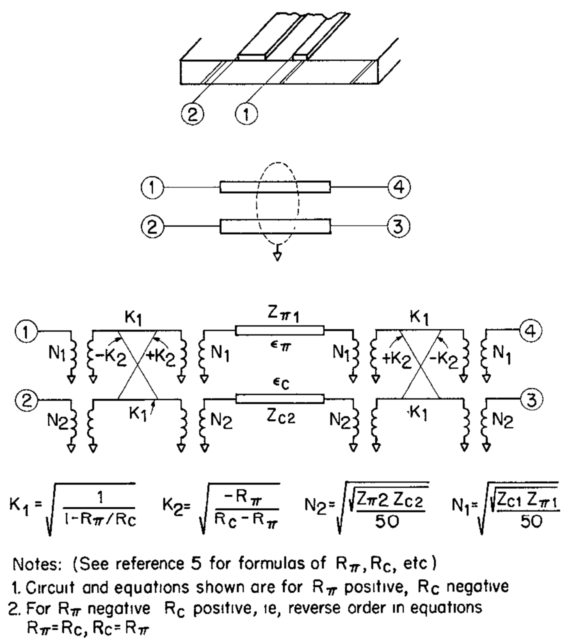

Figure 4b: Decoupled Equivalent Eigen-Circuit of Balun.

MIXER PERFORMANCE

Figure 6 shows conversion loss, VSWR, image rejection and LO to RF isolation at a constant LO power of +10 dBm. The image rejection at the band edges is only 15 dB but, this is sufficient to limit the RF preamplifiers, image noise contribution to only +0.13 dB. Figure 7 shows the midband conversion loss IP2 and IP3 as a function of LO power. The monolithic MESFETS used were fabricated at the Advanced Semiconductor Division of M/A-COM at Lowell, Massachusetts. Figure 8 illustrates the chip geometry. The MESFET was operated in the passive mode (i.e., zero drain current with a negative gate bias achieved by applying 2 volts to the source through the IF balun). The FET quad has an additional mixer circuit advantage of providing separate LO, RF and IF terminal pairs, whereas Schottky quads have only two isolated terminals. Toroidal, twisted 50 Ohm to 50 Ohm baluns were used to extract the IF and isolate the source bias voltage. High power level, narrow RF bandwidth, receiver applications are usually characterized by P(1 dB) and IP3 and IP2, whereas multioctave applications require knowledge of higher order single-tone products. Figure 9 shows these levels at -10 dBm RF input. Note that the theoretical relationship of -6 dB between the single-tone 2nd order product (2RF-LO) and two-tone levels of the same individual powers was observed. The corresponding difference between the two-tone IP3 and (3RF-LO) is 3:1 in voltage or approximately 9.5 dB less in power for the single-tone intermod. The LO input VSWR was considerably better than conventional MESFET mixers because the quadrature hybrid directed the normally high gate reflections to a terminated port port. The SSB noise figure of the mixer was within ±0.5 dB of the conversion loss.

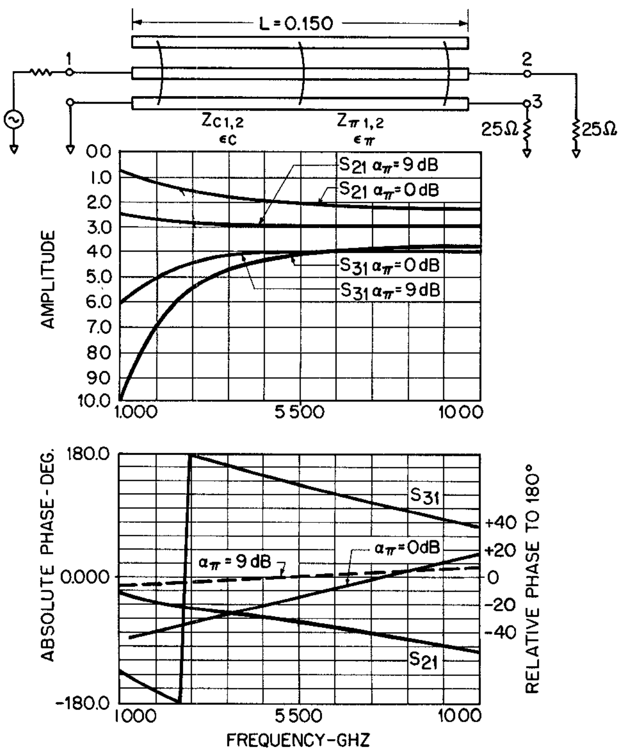

Figure 5: Phase and Amplitude Response of 3-Line Coplanar Balun.

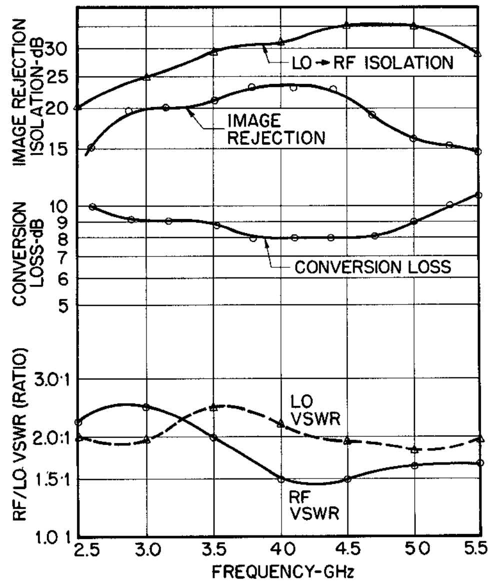

Figure 6: Performance of Passive MESFET Image Rejection Mixer at LO Power of +10 dBm.

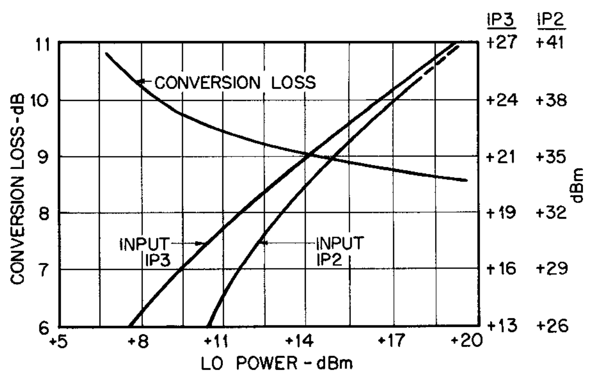

Figure 7: Conversion Loss and Two-Tone Input Intercept Points as a Function of LO Power.

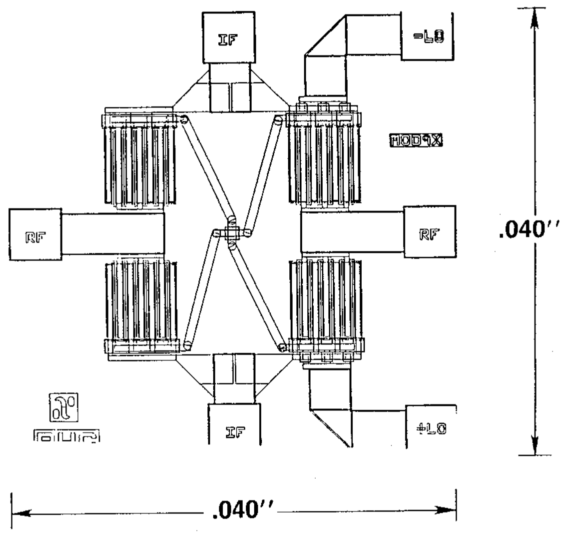

Figure 8: Layout of 1 μ MESFET Quad.

LO HARMONICS \ RF HARMONICS	1	2	3
3	27	44	56
2	34	52	52
1	0	42	56

Figure 9: Single-Tone Relative Intermodulation Levels at a GHz Input 100 MHz Output Using LO = +10 dBm, RF = -10 dBm.

CONCLUSIONS, FUTURE EFFECT

Further study about the relationship between the FET physical parameters and the IP3 level is ongoing. In addition, the merits of coplanar construction with MMIC mixer technology similar to that recently reported by Murphy (6) is being considered.

ACKNOWLEDGEMENTS

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